AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Currently Amended) A liquid crystal display (LCD) controller generating control signals for displaying in response to pixel data to display pictures on a liquid crystal panel having a plurality of pixels, the ~~liquid crystal display~~ LCD controller comprising:

a dithering pattern register section ~~for storing binary data of gray levels~~, comprising a first dithering pattern register for storing binary data of a gray level having a denominator value, wherein ~~a certain number of~~ the gray levels ~~have~~ has a same bit number as the denominator values of the first dithering pattern register ~~certain number of gray levels~~;

modular register counters for performing a counting operation to determine a binary value of a most significant bit ~~of each~~ of the gray levels in response to a frame clock, a line clock, and a pixel clock;

multiplexers for generating data patterns for the ~~respective~~ gray levels in accordance with an output of the respective modular register counters; and

a selection means for selecting and generating a corresponding bit of a data pattern corresponding to the pixel data provided on an LCD panel among the data patterns.

2. (Currently Amended) The ~~liquid crystal display~~ LCD controller of claim 1, wherein the dithering pattern register section forms dithering patterns using the same

bit number as the gray level of the denominator value of the first dithering pattern register ~~by dividing the gray levels into groups each having a same denominator value~~.

3. (Currently Amended) The ~~liquid crystal display~~ LCD controller of claim 1, wherein the dithering pattern register section is programmed to store the binary data as much as duty cycles for the ~~respective~~ gray levels using predetermined numbers as the denominator values of the gray levels.

4. (Currently Amended) The ~~liquid crystal display~~ LCD controller of claim 1, wherein each of the modular register counters comprises:

a modular frame counter for performing counting operation whenever a frame is changed in response to the frame clock;

a modular line counter for performing counting operation whenever a line of the frame is changed in response to the line clock;

a modular pixel counter for performing counting operation whenever a pixel of the line is changed in response to the pixel clock;

a next frame counter for generating a first update value to the modular frame counter in response to an output signal of the modular frame counter so that a current value in the modular frame counter is updated whenever the frame is changed;

a next line counter for generating a second update value in response to an output signal of the modular line counter;

a first multiplexer for selectively generating an initial value of the modular frame counter or the second update value provided from the next line counter to the modular line counter in response to a first selection signal;

a next pixel counter for generating a third update value whenever the pixel is changed in response to an output signal of the modular pixel counter; and

a second multiplexer for selectively generating the initial value of the modular frame counter, an initial value of the modular line counter, or the third update value provided from the next pixel counter to the modular pixel counter in response to a second selection signal.

5. (Currently Amended) The ~~liquid crystal display~~ LCD controller of claim 4, wherein the modular frame counter, the modular line counter, and the modular pixel counter perform the counting operations in synchronization with the frame clock, the line clock, and the pixel clock, respectively.

6. (Currently Amended) The ~~liquid crystal display~~ LCD controller of claim 4, wherein the next frame counter increases the first update value whenever the frame is changed, the next line counter increases the second update value whenever the line is changed, and the next pixel counter increases the third update value whenever the pixel is changed.

7. (Currently Amended) The ~~liquid crystal display~~ LCD controller of claim 1, wherein the modular frame counter, the modular line counter, and the modular pixel counter are initialized to a predetermined value whenever the frame is changed, the line is changed, and the pixel is changed, respectively.

8. (Currently Amended) À method for performing a dithering and frame rate control in a liquid crystal display (LCD) controller generating control signals for displaying in response to pixel data to display pictures on a liquid crystal panel having a plurality of pixels, the method comprising the steps of:

storing binary data of gray levels in a first, a second, a third and a fourth dithering pattern registers each register having a denominator value, wherein the gray levels using a same bit number as the denominator values of the first, second, third and fourth dithering pattern registers ~~gray levels~~;

performing a counting operation to determine a binary value of a most significant bit of the respective gray levels;

generating data patterns for the gray levels based on the binary value of the most significant bit; and

selecting and generating a corresponding bit of a data pattern corresponding to the pixel data.

9. (Currently Amended) The method of claim 8, wherein the step of performing the counting operation comprises the steps of:

performing a counting operation whenever a frame is changed in response to a frame clock;

performing a counting operation whenever a line of the frame is changed in response to a line clock;

performing a counting operation whenever a pixel of the line is changed in response to a pixel clock;

providing a first update value whenever the frame is changed to update a current value for the counting operation in response to the frame clock;

providing a second update value whenever the line is changed in response to a result of the counting operation in response to the line clock;

selectively providing an initial value for the counting operation in response to the frame clock or the second update value, to update a current value for the counting operation in response to the line clock;

providing a third update value in response to a result of the counting operation in response to the pixel clock whenever the pixel is changed; and

selectively providing the initial value for the counting operation in response to the frame clock, an initial value for the counting operation in response to the line clock, or the third update value, to update a current value for the counting operation in response to the pixel clock.

10. (Original) The method of claim 9, wherein the counting operations are performed in synchronization with the frame, line, and pixel clocks.

11. (Original) The method of claim 9, wherein the first update value is increased whenever the frame is changed, the second update value is increased whenever the line is changed, and the third update value is increased whenever the pixel is changed.

12. (Original) The method of claim 9, wherein the initial value for the counting operation in response to the frame clock is initialized to a predetermined value whenever the frame is changed.

13. (Original) The method of claim 9, wherein the initial value for the counting operation in response to the line clock is initialized to a predetermined value whenever the line is changed.

14. (Original) The method of claim 9, wherein an initial value for the counting operation in response to the pixel clock is initialized to a predetermined value whenever the pixel is changed.

15. (New) The LCD controller of claim 1, wherein the first dithering pattern register stores binary data of a gray level having a denominator value "7".

16. (New) The LCD controller of claim 1, wherein the dithering pattern register section further comprises:

a second, a third and a fourth dithering pattern register each for storing binary data of a gray level having a denominator value.

17. (New) The LCD controller of claim 16, wherein the second dithering pattern register stores binary data of a gray level having a denominator value "5", the third dithering pattern register stores binary data of a gray level having a denominator value "4", and the fourth dithering pattern register stores binary data of a gray level having a denominator value "3".